LISTING OF CLAIMS:

1. (Currently amended): An active matrix array device comprising:

a plurality of charging conductors;

a plurality of addressing conductors crossing the plurality of charging conductors; and

a plurality of matrix array elements, each matrix array element comprising a first switch having a control terminal coupled to an associated addressing conductor and a first data terminal coupled to an associated charging conductor, each matrix array element further comprising:

a first capacitive device coupled to a second data terminal of the first switch;

a second capacitive device coupled to the first capacitive device via a second switch having a control terminal responsive to a first enable signal, the second capacitive device having a smaller capacitance than the first capacitive device; ~~and~~

a third switch coupled between the first capacitive device and a potential source, the third switch having a control terminal coupled to the second capacitive device; and

a fourth switch coupled between the first capacitive device and the potential source, the fourth switch having a control terminal being responsive to a second enable signal.

2. (Canceled)

3. (Currently amended): An active matrix array device as claimed in claim 1 [[2]], wherein the third switch is coupled between the first capacitive device and the fourth switch.

4. (Currently amended): An active matrix array device as claimed in claim 1 [[2]] wherein the fourth switch is coupled between the first capacitive device and the third switch.

5. (Previously presented): An active matrix array device, comprising:

a plurality of charging conductors;

a plurality of addressing conductors crossing the plurality of charging conductors; and

a plurality of matrix array elements, each matrix array element comprising a first switch having a control terminal coupled to an associated addressing conductor and a first data terminal coupled to an associated charging conductor, each matrix array element further comprising:

a first capacitive device coupled to a second data terminal of the first switch;

a second capacitive device coupled to the first capacitive device via a second switch having a control terminal responsive to a first enable signal, the second capacitive device having a smaller capacitance than the first capacitive device; and

a third switch coupled between the first capacitive device and a potential source, the third switch having a control terminal coupled to the second capacitive device,

wherein the second capacitive device comprises a first sub-device and a second sub-device, the first sub-device having a first terminal coupled to a first enable conductor for providing the first enable signal and a second terminal coupled to a data terminal of the second switch, the second sub-device having a first terminal coupled to the data terminal of the second switch and a second terminal coupled to a second enable conductor for providing a second enable signal, and

wherein the third switch is coupled between the first capacitive device and the fourth switch.

6. (Original): An active matrix array device as claimed in claim 1, wherein the potential source is provided via the associated charging conductor.

7. (Currently amended): An active matrix array device as claimed in claim 1 [[2]], wherein each matrix array element further comprises a fifth switch having:

a control terminal responsive to a read-enable signal;

a first data terminal coupled between the third switch and the fourth switch; and

a further data terminal coupled to a read-out conductor.

8. (Original): An active matrix array device as claimed in claim 4, wherein the second switch is of a different channel type than the fourth switch, the control terminal of the second switch and the control terminal of the fourth switch being coupled to a common conductor.

9. (Currently amended): An electronic device comprising:

an active matrix array device comprising:

a plurality of charging conductors;

a plurality of addressing conductors crossing the plurality of charging conductors; and

a plurality of matrix array elements, each matrix array element comprising a first switch having a control terminal coupled to an associated addressing conductor and a first data terminal coupled to an associated charging conductor, each matrix array element further comprising:

a first capacitive device coupled to a second data terminal of the first switch;

a second capacitive device coupled to the first capacitive device via a second switch having a control terminal responsive to an enable signal, the second capacitive device having a smaller capacitance than the first capacitive device; ~~and~~

a third switch coupled between the first capacitive device and a potential source, the third switch having a control terminal coupled to the second capacitive device; and

a fourth switch coupled between the first capacitive device and the potential source, the fourth switch having a control terminal being responsive to a second enable signal;

the electronic device further comprising:

a first drive circuitry for driving a plurality of first signals onto the plurality of addressing conductors;

a second drive circuitry for driving a plurality of second signals onto the plurality of addressing conductors; and

a power supply for powering the first drive circuitry and the second drive circuitry.

10. (Original): A method of operating an active matrix array device having a plurality of matrix array elements including first and second capacitive devices, comprising:

storing a first voltage across the first capacitive device of a matrix array element;

storing the first voltage across the second capacitive device of the matrix element;

replacing the first voltage across the first capacitive device of the matrix array element with a second voltage; and

depending on the magnitude of the first voltage stored across the second capacitive device, enabling a current path between the first capacitive device and a potential source for replacing the second voltage across the first capacitive device with a third voltage.

11. (Previously presented): An active matrix array device as claimed in claim 1, wherein the control terminal of the third switch is a gate of a transistor.

12. (Previously presented): An electronic device as claimed in claim 9, wherein the control terminal of the third switch is a gate of a transistor.